REMARKS

Claims 1-32 are currently pending in the subject application and are presently under consideration. Claims 1, 6, 11, 16, 21, 26, 31 and 32 have been amended as shown on pp. 2-7 of the Reply. Claims 2, 7, 12, 17, 22 and 27 have been canceled. Claims 2, 7, 22 and 27 are allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, the corresponding independent claims have been amended to incorporate the limitations of the allowable dependent claims and the dependent claims have been canceled.

Applicants' representative thanks the Examiner for the courtesies extended during the teleconference of February 6, 2007.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claims 1, 3-5, 6 and 8-10 Under 35 U.S.C. §102(b)

Claims 1, 3-5, 6 and 8-10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Bishop *et al.* (US Patent 6,049,798). It is respectfully requested that this rejection should be withdrawn for at least the following reasons. Bishop *et al.* does not teach or suggest each and every element as set forth in the subject claims.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The claimed subject matter relates to systems and methods for determining real-time availability of computing resources. High-frequency interrupts *and/or* low priority threads are leveraged to more accurately determine which resources are available for computing. This provides a computing asset, such as a central processing unit (CPU) *and/or* a software application and the like, with a means to accurately compensate for resource utilization in order to increase its performance. In particular, independent claim 1 recites a performance monitoring

system, comprising: *a performance component that initiates at least one low-priority thread involving at least one computing resource,* ***the low-priority thread comprising at least one selected from the group consisting of a memory-intensive operation thread and a computationally-intensive operation thread****; and a monitoring component that obtains at least one performance parameter for the computing resource derived, at least in part, from the low-priority thread initiated by the performance component*. Bishop *et al.* does not expressly or inherently disclose the aforementioned novel aspects of applicants' claimed subject matter as recited in the subject claims.

Bishop *et al.* discloses a system resource monitor to capture a data processing system's internal resource utilization, such as memory, CPU, or peripheral device availability/utilization. The captured "state" of the data processing system's resources is maintained in real-time, while the impact on the system's performance in providing such information is kept to a minimum. This is accomplished through specialized device drivers coupled with a unique data reduction technique. Such techniques include filtering only events which are of interest and combining similarly related events to reduce data processing requirements. (*See* col. 3, lines 12-33).

In contrast, applicants' claimed subject matter discloses a performance monitoring system comprised of a performance monitoring component. The performance monitoring component interfaces with a CPU. The performance component is comprised of a low-priority thread component. The low-priority thread component initiates threads in the CPU that are memory-intensive *and/or* computationally-intensive operations. The optional performance optimizer component can interface with the low-priority thread component to sufficiently task the CPU for performance optimizing. Performance *and/or* resource availability is disseminated directly to computing assets (*e.g.*, CPUs, software applications, operating systems, *etc.*) *via* the low-priority thread component.

Thus, instead of letting an operation system run an idle loop, at least one thread of a very low priority is initiated so that there is only one such thread running on each logical/physical CPU. Each such thread, optimally, executes computationally- and memory-intensive code (*e.g.*, each thread runs a memory verification test which satisfies both conditions). Since these threads are of a very low priority, for example, one point above system idle, the threads do not typically prevent regular process threads from executing. And, because priority of these threads is generally just above system idle code, these threads gain control only when there are no other

higher priority executable threads/processes. In this way, the low-priority threads essentially substitute for the system idle thread. (*See* pg. 11, line 10-pg. 12, line 9). Bishop *et al.* does not expressly or inherently disclose a system that utilizes *…a performance component that initiates at least one low-priority thread involving at least one computing resource,* ***the low-priority thread comprising at least one selected from the group consisting of a memory-intensive operation thread and a computationally-intensive operation thread….*** Bishop *et al.* simply provides a system resource monitor that captures a data processing system's internal resource utilization *via* specialized device drivers coupled with a unique data reduction technique.

In view of at least the above, it is readily apparent that Bishop *et al.* fails to expressly or inherently disclose applicants' claimed subject matter as recited in independent claims 1 and 6 (and claims 3-5 and 8-10 which respectively depend there from). Accordingly, it is respectfully requested that these claims be deemed allowable.

II. Rejection of Claims 11, 13-16, 18-20 and 32Under 35 U.S.C. §102(b)

Claims 11, 13-16, 18-20 and 32 stand rejected under 35 U.S.C. §102(b) as being anticipated by Berc *et al.* (US Patent 5,796,939). It is respectfully requested that this rejection should be withdrawn for at least the following reasons. Berc *et al.* does not teach or suggest each and every element as set forth in the subject claims.

As stated *supra*, the claimed subject matter relates to systems and methods for determining real-time availability of computing resources. High-frequency interrupts *and/or* low priority threads are leveraged to more accurately determine which resources are available for computing. In particular, independent claim 11 recites a performance monitoring system, comprising: ***a performance component that initiates at least one high-frequency interrupt involving at least one computing resource, the high-frequency interrupt comprising an interrupt with a frequency of at least approximately 300 Hertz****; and a monitoring component that obtains at least one performance parameter for the computing resource derived, at least in part, from the high-frequency interrupt initiated by the performance component*. Berc *et al.* does not expressly or inherently disclose the aforementioned novel aspects of applicants' claimed subject matter as recited in the subject claims.

Berc *et al.* discloses an apparatus for collecting performance data in a computer system. The computer system includes a plurality of processors for concurrently executing instructions of

a program. The apparatus comprises a plurality of sets of performance counters. There is one set of performance counters coupled to each processor. The performance counters are for storing performance data generated by each processor while executing the instructions. (*See* col. 1, line 64-col. 2, line 5).

In contrast, applicants' claimed subject matter discloses a performance monitoring system comprised of a performance component and a monitoring component. The performance component interfaces with a CPU. The performance component initiates at least one high-frequency interrupt involving at least one computing resource. By utilizing an instance of the present invention, high-frequency interrupts (*e.g.*, approximately 300 Hertz or greater) are sent to the CPU so that it determines at a much higher frequency whether or not an application is running and, therefore, utilizing CPU resources. In the presently claimed subject matter, the system can provide checks approximately every 1 millisecond or quicker and, thus, reveal that the media server is utilizing CPU resources. (*See* pg. 13, lines 22-27). Berc *et al.* does not expressly or inherently disclose a system that utilizes …***a performance component that initiates at least one high-frequency interrupt involving at least one computing resource, the high-frequency interrupt comprising an interrupt with a frequency of at least approximately 300 Hertz***…. Berc *et al.* simply provides an interrupt handler that samples the performance data of the processor in response to interrupts, wherein the interrupting rate can be fixed or variable.

In view of at least the above, it is readily apparent that Berc *et al.* fails to expressly or inherently disclose applicants' claimed subject matter as recited in independent claims 11, 16 and 32 (and claims 13-15, 18 and 19-20 which respectively depend there from). Accordingly, it is respectfully requested that these claims be deemed allowable.

III. Rejection of Claims 12 and 17 Under 35 U.S.C. §103(a)

Claims 12 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Berc *et al.* as applied to claim 11 or 16 above. Claims 12 and 17 have been canceled, as such the rejection is moot and should be withdrawn.

IV. Rejection of Claims 21 and 23-31 Under 35 U.S.C. §103(a)

Claims 21 and 23-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Berc *et al.* in view of Bishop *et al.* It is respectfully requested that this rejection should be

withdrawn for at least the following reasons. Berc *et al.* and Bishop *et al.*, individually or in combination, do not teach or suggest each and every element as set forth in the subject claims.

> To reject claims in an application under §103, an examiner must show an unrebutted *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP §706.02(j). The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicants' disclosure. *See In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

As stated *supra*, the claimed subject matter relates to systems and methods for determining real-time availability of computing resources. High-frequency interrupts *and/or* low priority threads are leveraged to more accurately determine which resources are available for computing. In particular, independent claim 21 recites a performance monitoring system, comprising: *a performance component that initiates at least one low-priority thread involving at least one computing resource and at least one high-frequency interrupt involving at least one computing resource,* ***wherein the low-priority thread comprising at least one selected from the group consisting of a memory-intensive operation thread and a computationally-intensive operation thread****; and a monitoring component that obtains at least one performance parameter for the computing resource derived, at least in part, from at least one selected from the group consisting of the low-priority thread and the high-frequency interrupt initiated by the performance component*. The cited art, individually or in combination, fails to teach or suggest such aspects of the claimed subject matter.

Berc *et al.* discloses an apparatus for collecting performance data in a computer system. The computer system includes a plurality of processors for concurrently executing instructions of a program. The apparatus comprises a plurality of sets of performance counters. There is one set of performance counters coupled to each processor. The performance counters are for storing performance data generated by each processor while executing the instructions. (*See* col. 1, line

64-col. 2, line 5). The Examiner states that Berc *et al.* does not teach a performance component that initiates at least one low priority thread. (*See* Office Action dated 12-27-06, pg. 6).

Bishop *et al.* does not cure the deficiencies of Berc *et al.* with respect to independent claim 21, Bishop *et al.* discloses a system resource monitor to capture a data processing system's internal resource utilization, such as memory, CPU, or peripheral device availability/utilization. The captured "state" of the data processing system's resources is maintained in real-time, while the impact on the system's performance in providing such information is kept to a minimum. This is accomplished through specialized device drivers coupled with a unique data reduction technique. Such techniques include filtering only events which are of interest and combining similarly related events to reduce data processing requirements. (*See* col. 3, lines 12-33).

In contrast, applicants' claimed subject matter discloses a performance monitoring system comprised of a performance monitoring component. The performance component is comprised of a low-priority thread component. The low-priority thread component initiates threads in the CPU that are memory-intensive *and/or* computationally-intensive operations. The optional performance optimizer component can interface with the low-priority thread component to sufficiently task the CPU for performance optimizing. Performance *and/or* resource availability is disseminated directly to computing assets (*e.g.*, CPUs, software applications, operating systems, *etc.*) *via* the low-priority thread component.

Thus, instead of letting an operation system run an idle loop, at least one thread of a very low priority is initiated so that there is only one such thread running on each logical/physical CPU. Each such thread, optimally, executes computationally- and memory-intensive code (*e.g.*, each thread runs a memory verification test which satisfies both conditions). Since these threads are of a very low priority, for example, one point above system idle, the threads do not typically prevent regular process threads from executing. (*See* pg. 11, line 10-pg. 12, line 9). Bishop *et al.* does not expressly or inherently disclose a system that utilizes *…a performance component that initiates at least one low-priority thread involving at least one computing resource and at least one high-frequency interrupt involving at least one computing resource,* ***the low-priority thread comprising at least one selected from the group consisting of a memory-intensive operation thread and a computationally-intensive operation thread….*** Bishop *et al.* simply provides a system resource monitor that captures a data processing system's internal resource utilization *via* specialized device drivers coupled with a unique data reduction technique.

In view of the aforementioned deficiencies of the cited art, it is respectfully submitted that this rejection be withdrawn with respect to independent claims 21, 26 and 31 (and claims 23-25 and 27-30 which respectively depend there from).

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [MSFTP547US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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